WAFER LEVEL PACKAGE FOR PRODUCING CHIP SIZE PACKAGES AND METHOD OF FABRICATING THE SAME

A wafer level package for producing chip size packages is provided. The wafer level package of the present invention includes a plurality of chips on a surface of a wafer having trenches running through, each trench is formed between the chips. A filling material is filled in the trenches. Metal pads are formed on the surface of the wafer, a photosensitive polymer layer is formed on the surface of the wafer and exposing the metal pads. A first conductive layer is formed on the metal pads within the photosensitive polymer layer. A circuit distribution pattern is formed on the top of the photosensitive polymer layer and the first conductive layer. A protection layer is covered on the circuit distribution pattern, the photosensitive polymer layer, and a portion of the circuit distribution pattern is exposed. Conductive bumps are formed on the exposed circuit distribution pattern.